PATENT ABSTRACTS OF JAPAN

(54)TECHNIQUE FOR ANALYZING PARTIAL DIFFERENTIAL EQUATION BY FINITE ELEMENT METHOD
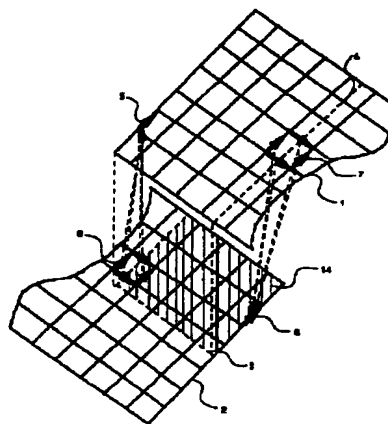
(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the distortion of an element and to reduce an analysis error by allowing the partial overlapping of elements and prevent simultaneous equations from being peculiar by transmitting the data of the overlapped part with each other.

SOLUTION: Space is divided into an element 1 and an element 2 and an element division is performed so that each element may overlap with each other. The vector 5 on the boundary of the boundary 1 of the element 1 is interporated by using the vector 8 in the interior of the element 2 and is used as the boundary value of the element 1. The vector 6 on the boundary of the element 2 is interporated by using the vector 5 in the interior of the element 1 and is used as the boundary value of the element 2. The direction of the interporated vector is not matched with the direction of the side element which is used as the boundary value. In order to take out the component of the side element, the inner product of the side direction vector (the covariant vector or the contravariant vector of the side is used according to the way of defining an unknown number) and the interporated vector is taken. In this way, the component of the vector along the side is obtained. Thus, simultaneous equations become regular and a solution can be obtained by connecting the element 1 and the element 2 by data.

(54) NUMERICAL VALUE ANALYZING DEVICE

(57) Abstract:

PURPOSE: To shorten the calculation time by directly executing numerical analysis of a differential equation by hardware and simplifying the processing before execution of operation to reduce error.

CONSTITUTION: The numerical analysis calculation work of a given Poisson's equation is executed by chips, namely, hardware. With respect to the work of one chip, values $\psi(i,j)$ are taken from four peripheral chips (i,j) and an average value is obtained, and a correction value $h^2\rho(i,j)$ recorded in the chip itself is subtracted from said obtained average value to obtain a value, and this value is stored in a certain address. Chips which perform this work are arranged at a pitch (h) and the number of prepared chips corresponds to the number of mesh points, and all chips are operated in parallel. By this constitution, the compile link processing like translation or linkage editing before execution is eliminated, and error is reduced because the preprocessing is simple, and processings of a controller and a main memory are reduced, and the calculation time is shortened.

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \rho(x,y)$$